Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.020”**

**.020”**

**NO**

**BOND**

**BOND PAD**

**.015”**

**.007”**

\***DO NOT BOND TO CENTER AREA\***

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .015” X .015” (See above)**

**Backside Potential: Cathode**

**Mask Ref: ZAB**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 9/1/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS: .008” P/N:1N5523B**

**DG 10.1.2**

#### Rev B, 7/19/02